CLAIMS

What is claimed is:

1. An interposer to couple a die to a substrate and comprising:

a capacitor having first and second terminals;

a first plurality of lands on a first surface thereof, including a first land coupled to the first terminal and a second land coupled to the second terminal; and

a second plurality of lands on a second surface thereof, including a third land coupled to the first terminal and a fourth land coupled to the second terminal.

2. The interposer recited in claim 1 wherein the first and second lands are positioned to be coupled to corresponding power supply nodes of the die, and wherein the third and fourth nodes are positioned to be coupled to corresponding power supply nodes of the substrate.

3. The interposer recited in claim 1 wherein the first and second lands are coupled to the first and second terminals, respectively, of the capacitor by a conductive path that comprises at least one via, and wherein the third and fourth lands are coupled to the first and second terminals, respectively, of the capacitor by a conductive path that comprises at least one additional via.

4. The interposer recited in claim 3 wherein the at least one via and the at least one additional via are located at an interior region of the interposer.

5. The interposer recited in claim 3 wherein the at least one via and the at least one additional via are located at a peripheral region of the interposer.

6. The interposer recited in claim 1 wherein the capacitor comprises at least one high permittivity layer.

7. The interposer recited in claim 1 wherein the capacitor comprises a plurality of high permittivity layers.

8. The interposer recited in claim 7 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

9. The interposer recited in claim 1 wherein the capacitor comprises at least one embedded discrete capacitor.

10. The interposer recited in claim 1 wherein the first plurality of lands comprises a fifth land positioned to be coupled to a corresponding signal node of the die, and wherein the second plurality of lands comprises a sixth land positioned to be coupled to a corresponding signal node of the substrate.

11. The interposer recited in claim 10 wherein the fifth and sixth lands are coupled by a conductive path that comprises at least one via.

12. An electronic assembly comprising:

a die comprising first and second power supply nodes;

a substrate having third and fourth power supply nodes; and

an interposer coupling the die to the substrate and comprising:

a capacitor having first and second terminals;

a first plurality of lands on a first surface thereof, including a first land coupled to the first power supply node and the first terminal, and further

including a second land coupled to the second power supply node and the second terminal; and

a second plurality of lands on a second surface thereof, including a third land coupled to the third power supply node and the first terminal, and further including a fourth land coupled to the fourth power supply node and the second terminal.

13. The electronic assembly recited in claim 12 wherein the capacitor comprises a plurality of high permittivity layers.

14. The electronic assembly recited in claim 13 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

15. The electronic assembly recited in claim 12 wherein the capacitor comprises at least one embedded discrete capacitor.

16. An electronic system comprising an electronic assembly comprising:

a die comprising first and second power supply nodes;

a substrate having third and fourth power supply nodes; and

an interposer coupling the die to the substrate and comprising:

a capacitor having first and second terminals;

a first plurality of lands on a first surface thereof, including a first land coupled to the first power supply node and the first terminal, and further including a second land coupled to the second power supply node and the second terminal; and

a second plurality of lands on a second surface thereof, including a third land coupled to the third power supply node and the first terminal, and further including a fourth land coupled to the fourth power supply node and the second terminal.

17. The electronic system recited in claim 16 wherein the capacitor comprises a plurality of high permittivity layers.

18. The electronic system recited in claim 17 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

19. The electronic system recited in claim 16 wherein the capacitor comprises at least one embedded discrete capacitor.

20. A data processing system comprising:

a bus coupling components in the data processing system;

a display coupled to the bus;

external memory coupled to the bus; and

a processor coupled to the bus and comprising an electronic assembly including:

a die comprising first and second power supply nodes;

a substrate having third and fourth power supply nodes; and

an interposer coupling the die to the substrate and comprising:

a capacitor having first and second terminals;

a first plurality of lands on a first surface thereof, including a first land coupled to the first power supply node and the first terminal, and further

including a second land coupled to the second power supply node and the second terminal; and

a second plurality of lands on a second surface thereof, including a third land coupled to the third power supply node and the first terminal, and further including a fourth land coupled to the fourth power supply node and the second terminal.

21. The data processing system recited in claim 20 wherein the capacitor comprises a plurality of high permittivity layers.

22. The data processing system recited in claim 21 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

23. A method for making an interposer to couple a die to a substrate, the method comprising:

forming within a multilayer ceramic structure at least one capacitor having first and second terminals;

forming in the structure first and second power supply nodes;

forming a first plurality of lands on a first surface of the structure, including a first land coupled to the first terminal and to the first power supply node, and a second land coupled to the second terminal and to the second power supply node, wherein the first and second lands are positioned to be coupled to first and second power supply nodes of the die; and

forming a second plurality of lands on a second surface of the structure, including a third land coupled to the first terminal and to the first power supply node, and a fourth land coupled to the second terminal and to the second power

supply node, wherein the third and fourth lands are positioned to be coupled to first and second power supply nodes of the substrate.

24. The method recited in claim 23 wherein the at least one capacitor is formed of a plurality of high permittivity layers.

25. The method recited in claim 24 wherein the at least one capacitor is formed of a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

26. The method recited in claim 23 wherein the at least one capacitor is formed of at least one embedded discrete capacitor.

27. A method of making an electronic assembly comprising:

providing a die having first and second power supply nodes;

providing an interposer comprising:

at least one capacitor having first and second terminals; and

a first plurality of lands on a first surface thereof including a first land coupled to the first terminal, and a second land coupled to the second terminal; and

a second plurality of lands on a second surface thereof including a third land coupled to the first terminal, and a fourth land coupled to the second terminal;

providing a substrate comprising third and fourth power supply nodes;

coupling the first and second lands to the first and second power supply nodes; and

coupling the third and fourth lands to the third and fourth power supply nodes.

28. The method recited in claim 27 wherein the at least one capacitor is formed of a plurality of high permittivity layers.

29. The method recited in claim 28 wherein the at least one capacitor is formed of a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

30. The method recited in claim 27 wherein the at least one capacitor is formed of at least one embedded discrete capacitor.